IN THE CLAIMS

Please add the following new claims:

35. (New) A method comprising:

receiving a read signal;

coupling a pass circuit between an internal node and a pin of an integrated circuit;

resetting the pass circuit with a reset circuit based on a first state of the read signal; and

passing the voltage from the internal node to the pin based on a second state of the read signal.

36. (New) The method of claim 35, wherein passing the voltage from the internal node includes driving a control node connected to the pass circuit to a first voltage based on the second state of the read signal.

37. (New) The method of claim 36, wherein driving includes passing an oscillating signal to the pass circuit.

38. (New) The method of claim 36, wherein resetting the pass circuit includes driving the control node to a second voltage based on the first state of the read signal.

39. (New) The method of claim 38, wherein resetting the pass circuit includes driving the control node to ground.

40. (New) A method comprising:

receiving a read signal;

coupling a pass circuit between an internal node and a pin of an integrated circuit;

applying an applied voltage to the pin;

resetting the pass circuit with a reset circuit based on a second state of the read signal; and

passing the applied voltage from the pin to the internal node based a second state of the

read signal.

41. (New) The method of claim 40, wherein passing the voltage from the pin includes driving a control node connected to the pass circuit to a first voltage based on the second state of the read signal.

42. (New) The method of claim 41, wherein driving includes passing an oscillating signal to the pass circuit.

43. (New) The method of claim 41, wherein resetting the pass circuit includes driving the control node to a second voltage based on the first state of the read signal.

Cont.

44. (New) The method of claim 43, wherein resetting the pass circuit includes driving the control node to ground.

45. (New) A method comprising:

receiving a read signal;

passing a voltage between an internal node and an access pin based on the first signal level of the read signal; and

isolating the access pin from the internal node based on a second signal level of the read signal.

46. (New) The method of claim 45, wherein passing a voltage includes pulling a control voltage of a control node to a first voltage level based on the first signal level of the read signal.

47. (New) The method of claim 46, wherein isolating the access pin includes pulling a control voltage of a control node to a second voltage level based on the second signal level of the read signal.

48. (New) The method of claim 45, wherein passing a voltage includes:
activating a control device connecting between the internal node and a pass node; and
activating a pass device connecting between the pass node and the access pin.

49. (New) The method of claim 48, wherein isolating the access pin includes deactivating the pass device.

50. (New) The method of claim 49, wherein isolating the access pin includes deactivating the control device.

51. (New) The method of claim 50, wherein isolating the access pin includes connecting the pass node to ground.

C' Cont.

52. (New) The method of claim 45, wherein isolating the access pin includes disabling a pass circuit connected between the access pin and the internal node.

53. (New) The method of claim 45, wherein isolating the access pin includes disconnecting a pass circuit connected to the access pin from a pass control circuit connected to the internal node.

54. (New) The method of claim 45, wherein isolating the access pin includes disconnecting a first terminal of a pass device connected to the access pin from a second terminal of the pass device connected to the internal node.

55. (New) The method of claim 45, wherein isolating the access pin includes cutting off a conduction channel between a source of a pass transistor connected to the access pin and a drain of the pass transistor.

56. (New) A method comprising:
receiving a read signal;

passing an internal voltage from an internal node to an access pin based on a first signal level of the read signal; and

isolating the access pin from the internal node based on a second signal level of the read signal.

57. (New) The method of claim 56, wherein passing an internal voltage includes:

passing the internal voltage to a pass node; and

passing the internal voltage from the pass node to the access pin.

58. (New) The method of claim 57, wherein:

passing the internal voltage to a pass node is performed by a pass control circuit connecting between the internal node and the pass node; and

passing the internal voltage from the pass node to the access is performed by a pass circuit connecting between the pass node and the access pin.

C' cont.

59. (New) The method of claim 57, wherein isolating the access pin includes pulling a voltage of the pass node to ground.

60. (New) The method of claim 56, wherein passing an internal voltage includes:

activating a control device connecting between the internal node and a pass node; and

activating a pass device connecting between the pass node and the access pin.

61. (New) The method of claim 60, wherein isolating the access pin includes deactivating the pass device.

62. (New) The method of claim 61, wherein isolating the access pin includes deactivating the control device.

63. (New) The method of claim 62, wherein isolating the access pin includes connecting the pass node to ground.

64. (New) A method comprising:

receiving a read signal;

passing a pin voltage from an access pin to an internal node based on a first signal level of the read signal; and

isolating the access pin from the internal node based on a second signal level of the read signal.

65. (New) The method of claim 64, wherein passing a pin voltage includes:

turning on a control transistor connecting between the internal node and a pass node; and

turning on a pass transistor connecting between the pass node and the access pin.

Cont.

66. (New) The method of claim 65, wherein isolating the access pin includes turning off the pass transistor.

67. (New) The method of claim 66, wherein isolating the access pin includes turning off the control transistor.

68. (New) The method of claim 67, wherein isolating the access pin includes connecting the pass node to ground.

69. (New) A method comprising:

receiving a read signal;

activating a control device during a first signal level of the read signal to pass a voltage between an internal node inside a memory device and a pass node inside the memory device;

activating a pass device during the first signal level of the read signal to pass the voltage between the pass node and an input/output pin of the memory device;

deactivating a reset circuit during the first signal level of the read signal to isolate the pass node from ground;

deactivating the control device during a second signal level of the read signal;

deactivating the pass device during the second signal level of the read signal; and

activating the reset circuit during the second signal level of the read signal to connect the pass node to ground.

70. (New) The method of claim 69, wherein activating a control device during a first signal level of the read signal to pass a voltage between an internal node inside a memory device and a pass node inside the memory device includes:

passing an internal voltage from the internal node to the pass node.

C' cont

71. (New) The method of claim 70, wherein activating a pass device during the first signal level of the read signal to pass the voltage between the pass node and an input/output pin of the memory device includes:

passing the internal voltage from the pass node to the input/output pin.

72. (New) The method of claim 71, wherein activating a control device during a first signal level of the read signal to pass a voltage between an internal node inside a memory device and a pass node inside the memory device includes:

passing an applied voltage from the pass node to the internal node.

73. (New) The method of claim 72, wherein activating a pass device during the first signal level of the read signal to pass the voltage between the pass node and an input/output pin of the memory device includes:

passing the applied voltage from the input/output pin to the pass node.